

**REMARKS**

Claims 5-7 are pending in the present application. Claim 5 has been amended to put it into a form similar to that of claim 1 of 6,515,543. Claim 7 has been amended to correct an inadvertent error as pointed out in the Office Action. Reconsideration of the rejection of the application is respectfully requested in view of the following remarks.

**Rejections Under 35 U.S.C. § 112, Second Paragraph**

Claim 7 was rejected under 35 U.S.C. § 112, second paragraph. Claim 7 has been amended to more clearly refer to biasing voltage in the transistor's active mode. In view of this amendment, reconsideration and withdrawal of the rejection of claim 7 under 35 U.S.C. § 112, second paragraph is respectfully requested.

**The Claims Are Allowable Over the Prior Art**

Claims 5-7 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,469,568 to Toyoyama et al. ("Toyoyama"). Claims 5-7 were also rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. 6,429,684 to Houston ("Houston"). Reconsideration of the rejection is respectfully requested in view of the following remarks.

First, with respect to Toyoyama, the application that issued as U.S. Patent No. 6,469,568 was filed on December 22, 2000. The present application claims priority to

U.S. Application Serial No. 09/475,648, filed on December 30, 1999. Since the application for Toyoyama was not filed in the U.S. prior to the filing date of the '648 application, it cannot be considered prior art under 35 U.S.C. § 102(e). Nonetheless, in Toyoyama, the gate voltage is shorted to the body of the transistor. There is nothing in Toyoyama that teaches or suggests the detection of that voltage and the application of a bias voltage to the body of the transistor based on that detected voltage as recited in the claims.

Independent claim 5 recites a transistor with a first terminal and a body. A voltage detector is also provided that is to detect the terminal voltage applied to the first terminal and apply a bias voltage to the body of the transistor based upon the detected terminal voltage. Also, a single source voltage is to be used to detect the voltage applied to the first terminal and to operate the transistor.

With respect to claim 5, Houston does not provide for a voltage detector to detect a terminal voltage applying a bias voltage to the body of the transistor based upon the detected voltage as recited in claim 5. In Houston, though the gate terminals of the transistors are coupled to the IN and /IN voltages, there is no disclosure in Houston concerning the detection of that voltage and the application of a bias voltage to the body of the transistor as recited in the claims.

Since features of the pending claims are missing from the Houston reference, reconsideration and withdrawal of the rejection of claims 5-7 under 35 U.S.C. § 102(e) is respectfully requested.

**Conclusion**

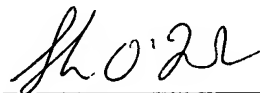
Applicant respectfully requests entry of the above amendments and favorable action in connection with this application.

The Examiner is invited to contact the undersigned to discuss any matter concerning this application.

The Office is hereby authorized to charge any fees required under 37 C.F.R. §§ 1.16 or 1.17 or credit any overpayment to Kenyon and Kenyon Deposit Account No. 11-0600.

Respectfully submitted,

KENYON & KENYON



---

Shawn W. O'Dowd  
Registration No. 34,687  
Attorney for Intel Corporation

Date: October 28, 2004

KENYON & KENYON  
1500 K Street, N.W.  
Suite 700  
Washington, D.C. 20005  
Ph.: (202) 220-4200  
Fax.: (202) 220-4201  
DC1-509716